Millimeter-Wave Device Technology

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Abstract—**We have investigated novel techniques for the fabrication of silicon IMPATT diodes for use at frequencies of 220 GHz and beyond. We report on diodes yielding 25 mW CW at 102 GHz with 2-percent conversion efficiency, and 16 mW CW at 132 GHz with 1-percent conversion efficiency. The basic techniques described are ion implantation, laser annealing, unique secondary-ion mass spectrometry (SIMS) profile diagnostics, and novel wafer thinning, yielding ultrathin, reproducible wafers. The utilization of these technologies, as they are further refined, can result in the development of silicon monolithic integrated sources.**

I. Introduction

In THE last two years, we have investigated and developed the technology base for silicon IMPATT diodes for use at frequencies of up to 220 GHz. An outgrowth of this effort has been the development of a novel device technology which facilitates simple, well-controlled processing procedures for the fabrication of ultrathin, IMPATT devices, with good heat sinking properties. The devices produced are capable of CW operation with 25-mW output power, at above 100 GHz, with a conversion efficiency of 2 percent. In our early work at 60 GHz [1], conventional p^+-n silicon diodes were developed, that yielded CW power output in excess of 500 mW at 6-percent efficiency. Most recently, our complementary (n^+-p) silicon IMPATT diodes operating at 132 GHz have yielded 16 mW with 1-percent conversion efficiency.

The work most relevant to our success includes our excellent impurity concentration profile and thickness control developed for multilayer vapor-phase expitaxial silicon devices, and our wafer thinning procedure developed for the fabrication of small-area ultrathin (2 μm) IMPATT diodes (Fig. 1). Our present device fabrication technology permits the fabrication of IMPATT devices for use at frequencies above 200 GHz, utilizing ion implantation and laser annealing.

This paper describes the development of a new technology which will result in the development of devices that operate at higher frequencies with increased efficiency. In addition, the possibility of developing monolithic integrated circuits in silicon using the new technology is brought out.

The RF impedance, the need for stringent impurity concentration profile control, ohmic contact resistance, and heat dissipation requirements, make the millimeter-wave IMPATT oscillator a device that requires a state-of-the-art technology for fabrication. These requirements were successfully met by using small-area ($<10^{-5}$ cm^2) single-drift and double-drift devices with ultrathin low-resistivity contacting layers to reduce both the thermal and the electrical series resistance. The use of ultrathin wafers (2–3 μm) also alleviates the problem of undesirable undercutting during the formation of the small-area mesas.

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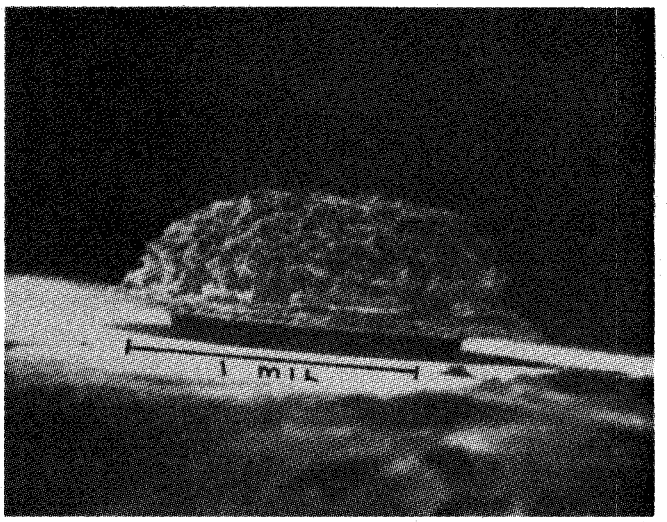

Fig. 1. View of the diode.

II. Vapor-Phase Silicon Epitaxial Multilayer IMPATT Diode Structures

We have successfully fabricated the following structure as shown in Fig. 2:

1) substrate: 3×10^{19} (arsenic doped);
2) first epifilm: 0.3 μm of 3×10^{17} (n) (arsenic doped);
3) second epifilm: 0.3 μm of 2×10^{17} (p) (boron doped).

An ion implantation (not shown) completes the double-drift IMPATT structure.

A. Deposition

Vapor-phase epitaxial-silicon single and multilayer IMPATT diode structures [2]–[5], as shown in Figs. 2 and 3, are deposited on a (111) oriented substrate, in a hydrogen atmosphere, using the conventional silane (SiH_4) decomposition method. All the silicon layers are deposited at a substrate temperature ranging from 1000°C to 1050°C.

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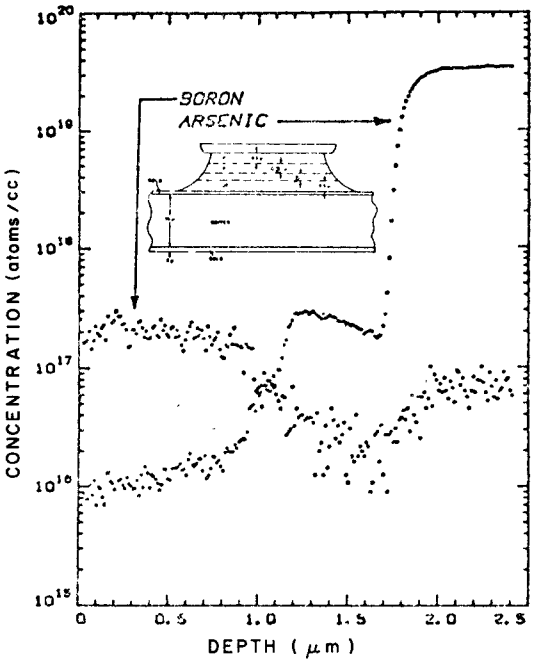

Fig. 2. SIMS depth profiles of epigrown n and p on n^+ arsenic-doped substrate.

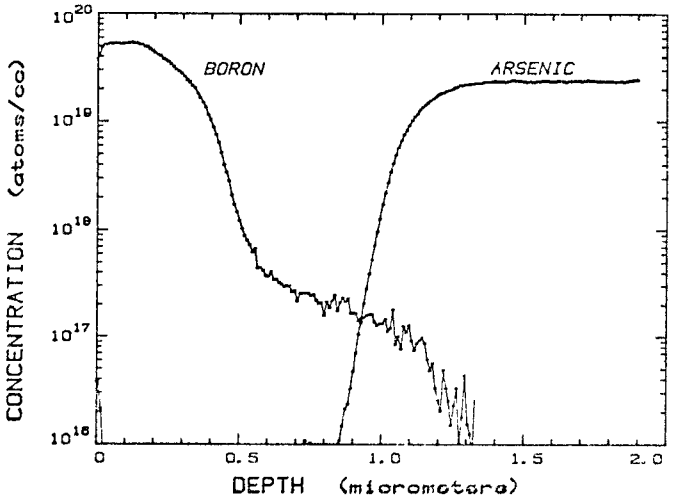

Fig. 3. SIMS depth profiles of epigrown p and ion-implanted p^+ and n^+ arsenic-doped substrate.

Diborane or arsine gas are introduced during the epitaxial growth process to achieve the desired impurity concentration in the respective layers.

B. Growth

The substrates' back surface and side edges were coated with 2000 Å of deposited oxide. The substrates were heated to approximately 1150°C and etched with HCl (1-percent HCl for 5 min). The temperature was then dropped to approximately 1050°C and the first epilayer was grown. The system was then purged of all reaction gases (at 1050°C) before the second epifilm was grown. The adjustment of crystal growth parameters, using impurity concentration profiles by secondary-ion mass spectrometry (SIMS), has led to sharp transitions (Fig. 4). The concentration varies from 3×10^{19} atoms/cm^3 in the substrate to 2×10^{17} atoms/cm^3 in the epitaxial layer over a distance of only 3000 Å.

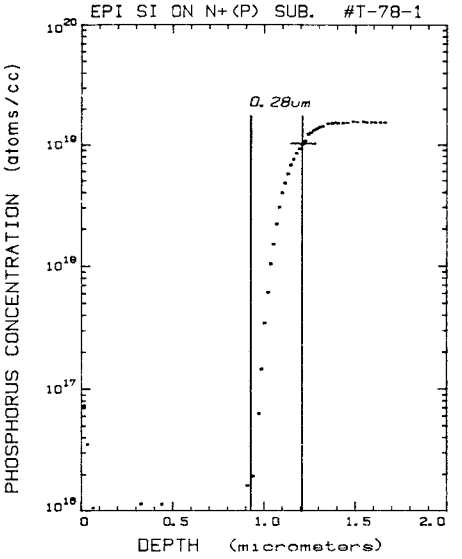

Fig. 4. Transition of epigrown n on n^+ substrate.

III. Device Fabrication by Ion Implantation and Laser Annealing

A. Single Drift

As discussed above, the conventional fabrication technique is via epitaxy. The n layer, followed by p and p^+ layers, are grown in succession upon an n^+ substrate which serves as a handle during the fabrication (this substrate is partially etched away just before the final Cr–Au metallization). When the design frequency of the IMPATT exceeds 140 GHz, the doping profile requirements (e.g., junction abruptness and uniform layer thickness) are difficult to meet using this epitaxial technique.

A novel application of both ion implantation and laser annealing techniques was first proposed [6] to achieve uniformity and reproducibility of the closely spaced junctions. The single-drift IMPATT was successfully processed as a vehicle for the more difficult double-drift structure. First, an n layer with doping concentration of about 5×10^{16} cm^{-3} is grown at 1050°C on a (111) oriented n^+ silicon substrate using conventional silane pyrolysis. The thickness of this n epilayer is 2 μm. Next, two ion implants are carried out under the following conditions:

1) n region: ^{31}P implant at 500 keV with a fluency of 1×10^{13} cm^{-2};
2) p^+ region: ^{11}B implant at 50 keV with a fluency of 2×10^{15} cm^{-2}.

Typical SIMS analyses of these implants are shown in Fig. 5(a)—before, and Fig. 5(b)—after annealing. After the above ion implants, the wafer can be either thermally annealed at 1000 °C for 15 min in dry N_2 (after depositing 0.5 μm SiO_2 as capping) or laser annealed.

The wafer is then metallized on the p^+ side with Cr–Au

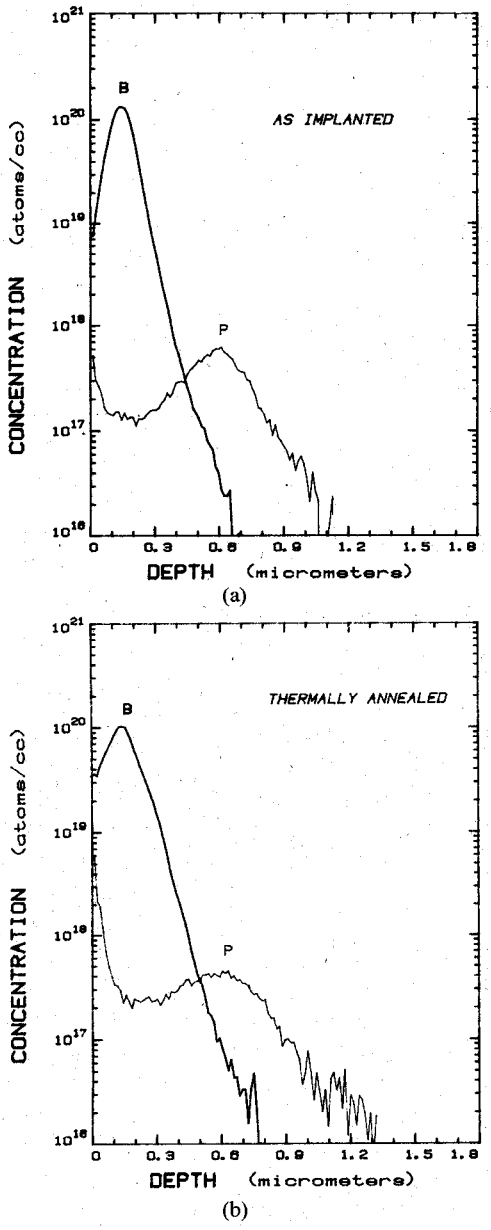

Fig. 5. Results (measured by SIMS) obtained (a) on implanting ^{31}P and ^{11}B in silicon; (b) after annealing, on implanting ^{31}P and ^{11}B in silicon.

and electroplated with 25-μm-thick copper to form the heat sink. Another layer of gold, 2 μm thick, can be plated upon the copper heat sink. This metallization also serves as a handle for subsequent processing. At this point, the n^+ silicon substrate can be completely or partially removed by the procedure for wafer thinning, described in the next section.

Next, the n^+ layer is formed by a 950 keV $^{31}P^+$ ion implant with a fluence of 3×10^{15} cm^{-2}. This implanted layer of 0.95-μm depth is then laser annealed. The laser annealing heats up only a 1-μm depth of the material at the surface for a very short time ($\sim$1 μs). Thus, there is no deleterious effect at the metal–silicon interface (2 μm away), and profile redistribution is minimized. The application of laser annealing here is unique, since, at this point in the processing sequence, the above device structure (with a metallic coating) cannot be thermally annealed.

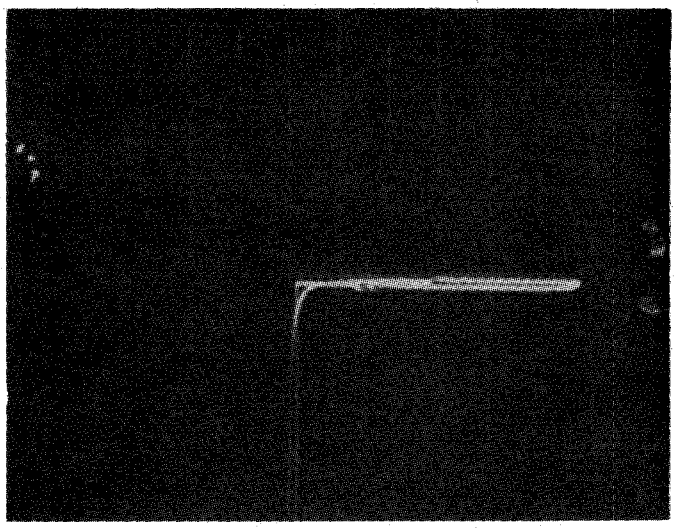

Fig. 6. I–V characteristics of a millimeter-wave IMPATT diode. (0.01 mA/vertical division; 2 V/horizontal division.)

The n^+ contact layer is first evaporated with Cr–Au. Then, an array of gold dots is electroplated through a photoresist mask. The unplated metallization is removed, and mesa diodes are formed by etching completely through the unplated area of the semiconductor layer. Finally, the diodes are separated; each diode, with its attached copper heat sink, is now ready to be tested. I–V characteristics are shown in Fig. 6.

B. Double-Drift Structures

For applications of the double-drift diode at around 140 GHz, a millimeter-wave IMPATT diode with symmetrical structure and total active layer thickness of 0.5 μm is desired. Such a device requires four implants instead of only three. The proposed device is to have a total thickness of 1.5 μm. Hence, an n epilayer of 1.5-μm thickness and doping concentration of 1×10^{16} cm^{-3} is first grown on an (111)-oriented n^+ silicon substrate. The doping concentration of the n epilayer is not critical in this case and can be varied within a factor of 2 or 3 without seriously affecting the final performance of the finished device. However, the thickness of the n epilayer should be carefully measured and controlled. The processing is essentially similar to that described in the previous section, except for the insertion of the 0.25-μm n layer by a $^{31}P^{++}$ ion implantation at 280 keV after the implant for the n^+ contact. The $^{31}P^{++}$ ion implant at 280 keV has the same penetration as a $^{31}P^+$ ion implant at 560 KeV, which is needed for the deep penetration. Both the n^+ and the n region are laser annealed (simultaneously) as described in the next section.

IV. Technology Specifics

A. Laser Annealing

Laser annealing was performed with a pulsed Nd:YAG laser [7], [25]. The laser beam has a pulsewidth of 15 ns and contains both the 1.06-μm and the 0.53-μm compo-

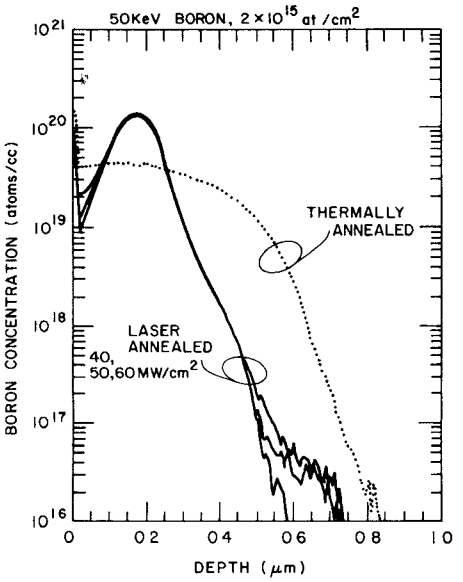

Fig. 7. Profile distribution determined by SIMS (laser as opposed to thermal annealing).

nents. This is achieved by passing the fundamental output of the two-stage pulsed Nd:YAG laser through a Type II KD*P crystal frequency doubler, which has a conversion efficiency of 30 percent. The dual output pulses are collinear and are optically scanned over the target wafer. The 0.53-μm component has a higher absorption coefficient in silicon. Electrons and holes generated by the 0.53-μm component enhance the absorption of energy from the 1.06-μm component, which penetrates deeper in silicon and is more suitable for annealing deep implants. The laser beam spot has a diameter of 6 mm, with ~50-percent overlap between adjacent spots. The pulsed laser is operated at a repetition rate of 10 pps.

Fig. 7 shows the profile distribution, determined by SIMS [8]–[10], of the ion implantation of 50-keV boron into a 10^{16} atoms/cm^3 As-doped epi-grown substrate. The ion-implantation fluency level determines the concentration profiles. The improvement accomplished by the use of laser annealing as opposed to thermal annealing is evident as the sharpness in the profile distribution increases with increasing pulse densities. The ability to obtain the concentration profile by SIMS diagnostics has enabled us to accurately determine the carrier profile resulting from the ion implantation and annealing processes.

B. Secondary-Ion Mass Spectrometry

We have built our own instrument [8] for performing SIMS. This instrument is particularly well suited for silicon device research because of its Cs^+ primary ion source and its ultrahigh vacuum capabilities. We have shown [9] how these attributes have enabled us to profile n type dopants (P and As) in Si, to concentrations down to less than one part per million atomic (ppma). This type of accuracy is normally impossible using a more traditional SIMS instrumentation. Furthermore, we have shown [10] how to depth-profile p and n type dopants simultaneously and thus determine electrical junction depths *directly* from the SIMS data. It is this unique capability which has been of most benefit to millimeter-wave device research. When fabricating double-drift diodes by ion implantation, the As-implanted dopant distribution can only be predicted. SIMS is used to measure accurately the p and n dopant distribution after thermal annealing, which is important because diffusion can often alter the profiles in an unpredictable manner, smearing together the very thin layers needed for high gigahertz operation. We have been successful in determining whether or not the implantation and diffusion steps have produced the desired doping profiles prior to the difficult and tedious steps needed to process the wafers into diodes. SIMS will be of even greater benefit with high-energy (exceeding 1 MeV) ion implantation coupled with laser annealing, because of the less precisely known ion ranges at these energy levels and, as yet, relatively unpredictable diffusion behavior with laser annealing.

C. Wafer Thinning

1)Conventional Technique:

1. Metallization with Cr–Au on the p^+ side serves as the handle.

2. A hole is opened in the center of the metallization to allow for light transmission measurement to evaluate wafer thickness.

3. The center of the wafer is chemically thinned to as low as 2 μm. The wafer is then supported by the remaining outside ring and the top metallization (with the hole).

The thickness of the n epi is then amenable to precision control and measurement.

2) Preferential Etching (n on n^+) [11]: An extensive investigation of a preferential silicon etch has been launched in order to enhance our capability to thin uniformly our substrates and remove selectively n^+ material from n.

TABLE I
ETCH RATES

Impurity concentration (atoms/cm^3)	Etched alone (μm/min)	With 10^{19} sample (μm/min)	With Au metallization (μm/min)	With Au metallization and 10^{19} sample (μm/min)
10^{13}	0.0005–0.0007	0.02	0.04	0.1–0.5
10^{17}	0.003–0.008	0.01	—	0.04
10^{19}	2.7–3.5	2.7–3.5		2.7–3.5

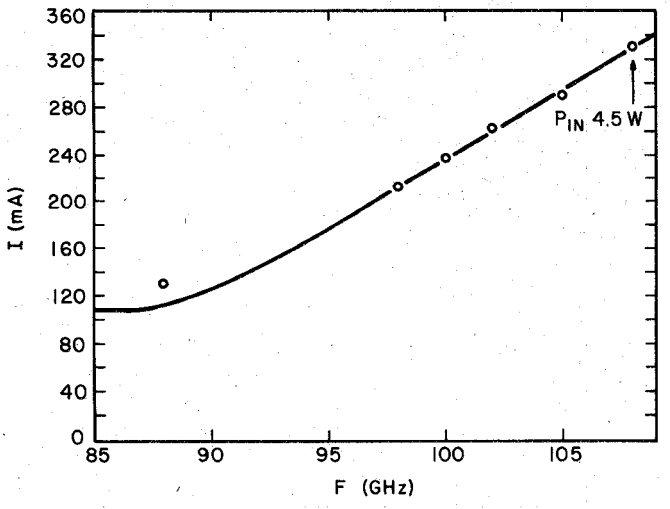

Fig. 8. DC supply current (I) versus IMPATT frequency (F).

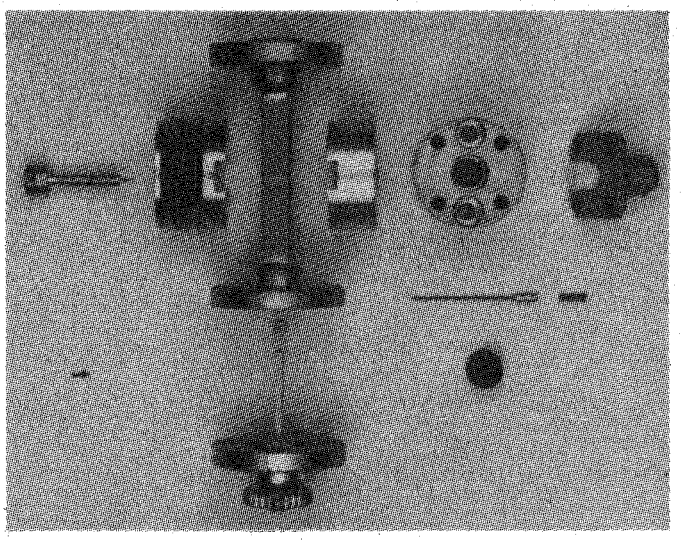

Fig. 9. Photograph of the disassembled oscillator circuit.

We have tested an $8CH_3COOH:3HNO_3:1HF$ solution on (111) orientation, n type wafers. Wafers with impurity concentrations of 10^{13}, 10^{17}, and 10^{19} atoms/cm^3 were used. Several major factors influenced the n etch rate: 1) etching two wafers of different impurity levels simultaneously; 2) the presence of gold metallization; and 3) uniformity of the crystal structure. The 10^{19} atoms/cm^3 (n^+) wafers were the least influenced by these factors, since these wafers etched relatively fast (between 2.7–3.5 μm/min). The etch rates of samples with impurity concentration of less than 10^{18} atoms/cm^3 (n) are significantly lower than 3 μm/min. Several examples of these effects are seen in Table I.

An epilayer of 1.5×10^{15} atoms/cm^3 (on a 10^{19} atom/cm^3 Au-backed substrate) yielded an etch rate of 0.89 μm per minute.

We have achieved repeatability by the careful control of various physical conditions such as total solution volume, temperature, and mix action. Muraoka *et al.* [11] were able to improve results substantially by introducing hydrogen peroxide. We expect this preferential etch to yield suitable etch-rate ratios of at least 10:1 under the worst conditions.

V. Reduced-Height Circuits (Above 140 GHz)

Reduced-height waveguide circuits [13]–[15], (Figs. 9 and 10) were used in evaluating the IMPATT diodes. The integrated heat sink IMPATT was mounted on top of a 16-mil-diameter post (Fig. 11) [16], and connected to a dc bias through a pressure-loaded p-i-n as shown in Fig. 10. A bandstop filter in the bias line was used to prevent RF leakage at the output frequency. At the end of the dc bias line (Fig. 9) an RF termination constructed of an insulating material providing high RF loss was used. Typical

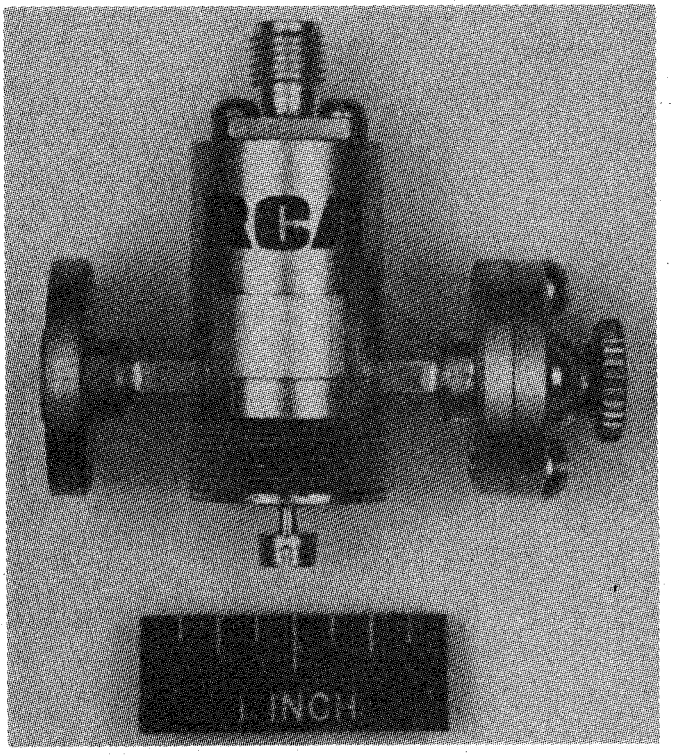

Fig. 10. Reduced-height waveguide circuit.

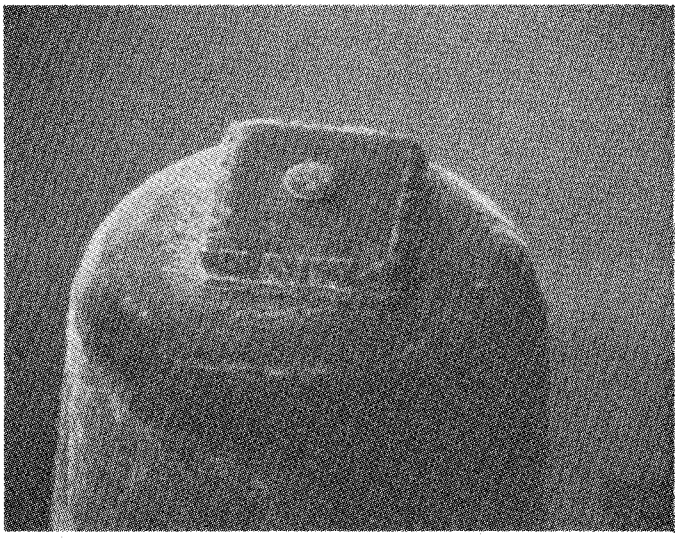

Fig. 11. Diode mounted on p-i-n.

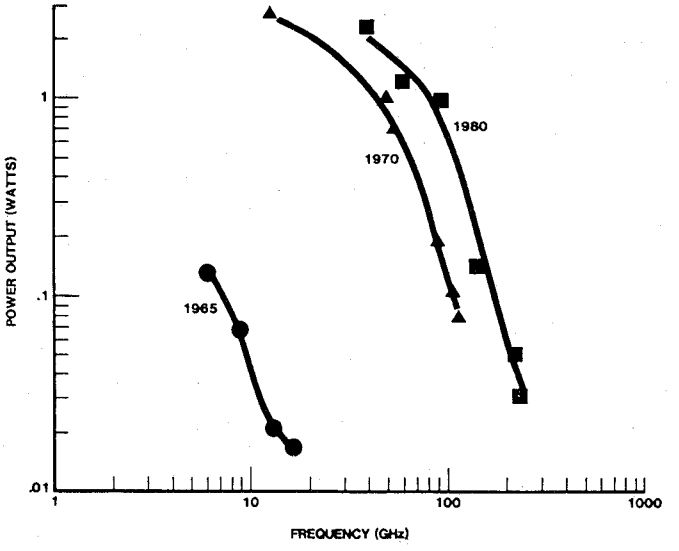

Fig. 12. Performance progress for state-of-the-art Si IMPATT diodes [17]–[24].

diode-operating conditions at above 100 GHz are $v_0 = 14.2$ V and $I_0 = 111$ mA. Device-circuit tuning capabilities are depicted in Fig. 8.

VI. Implication/Monolithic Silicon Integration

We believe that the technology base that we have developed will enable the fabrication of millimeter-wave IMPATT sources for operation at frequencies above 220 GHz, yielding better power and efficiency than are available in the state of the art. A technique explored in the early days of MIC technology was that of microstrip lines on silicon. In 1965, T. M. Hyltin of Texas Instruments showed impressive results using silicon of 1400-$\Omega \cdot$cm resistivity. In the MERA program [12], he proposed growing devices on high-resistivity material to integrate the circuits monolithically. This approach failed when it was found that the processing steps involved in the epitaxial growth significantly lowered the resistivity of the silicon. There now exist new ways to process silicon wafers, namely ion implantation and laser annealing, which do not require high temperatures. The active device can now be fabricated without degradation of the high-resistivity substrate needed for the passive network. These new techniques afford many new possibilities, particularly in the area of millimeter waves. The advantages of the monolithic integrated circuits technology include low production costs through batch processing, high reliability, and compact size. In light of the apparent saturation in both frequency and power output shown in Fig. 12, monolithic circuits using an improved technology show promise for the future.

VIII. Conclusions

We have examined a new technology which has enabled us to fabricate ultrathin IMPATT devices, with reported results that approximate those of the state of the art. The

basics of the techniques involved are as follows: 1) all ion-implantation; 2) laser annealing; 3) highly refined SIMS profile diagnostics; and 4) novel wafer-thinning techniques, leading to reproducible, uniform device layers. The promise of these techniques, as they are further refined, lies in the strong possibility of developing silicon monolithic integrated millimeter-wave circuits.

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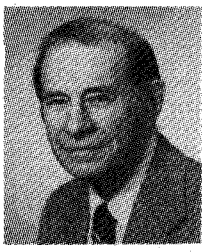
Mr. Rosen is a member of Tau Beta Phi, Sigma Xi, and the Association of Professional Engineers of British Columbia.

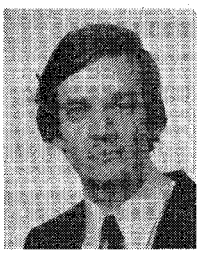


Martin Caulton (M'61–SM'65–F'80) received the B.S., M.S., and Ph.D. degrees, all in physics, from Rensselaer Polytechnic Institute, in 1950, 1952, and 1954, respectively. He completed his doctoral research at the Brookhaven National Laboratories in high-energy nuclear physics. From 1954 to 1955 he was a Fulbright scholar at the Imperial College of Science and Technology in London. In 1955, he joined the Technical Staff at Bell Telephone Laboratories working in research and development of low-noise microwave tubes. In 1958 he became Assistant Professor of Physics at Union College, Schenectady, New York.

He joined RCA Laboratories as a Member of Technical Staff, in 1960. There he engaged in research on microwave power tubes, multivelocity flow problems in electron beams and plasmas, and microwave solid-state devices. He has been directing projects in microwave integrated circuits

since 1966, and has authored numerous papers in this field. In 1968 and 1971 he was the recipient of RCA Laboratories' Achievement Awards for this work. He has worked on the basic design and measurement of microstrip circuits and integration methods based on the use of lumped elements for the miniaturization of high-power amplifiers and microwave circuits, including FET devices. He has coauthored a textbook, *Physical Electronics* (John Wiley & Sons, Inc., New York, 1967), and has also taught courses in microwaves and modern physics as Adjunct Professor of Electrical Engineering at Drexel Institute of Technology. In 1971–1972 he served as Visiting Professor at the Technion (Israel Institute of Technology) in Haifa, Israel.

From 1970 to 1975 Dr. Caulton served first as Cochairman and later as Chairman of the Committee on Microwave Integrated Circuits of IEEE's Microwave Theory and Techniques Society and was formerly an Associate Editor of *Transactions of Microwave Theory and Techniques*. He is a member of the American Physical Society and Sigma Xi.



Paul Stabile (S'75–M'79) received the B.E. degree in electrical engineering summa cum laude from Manhattan College in 1979. Afterward, he entered the Engineering Rotation Program at RCA. His assignments included microwave amplifier design, digital circuit development, and a study of VLSI computer aided design techniques.

In October 1979, he joined RCA Laboratories, where he is presently an Associate Member of Technical Staff. There he has been engaged in research of high power, low-frequency p-i-n diodes, and silicon millimeter wave devices, and integrated circuits. He is also the author of several technical papers.

Mr. Stabile is a member of Eta Kappa Nu, Tau Beta Pi, and Epsilon Sigma Pi of Manhattan College.

Anna M. Gombar was born in Hungary. After attending the Technical University in Budapest, she came to the United States in 1956.

In 1960 she began textile research at FMC in Princeton, NJ. Transfering to RCA Laboratories in 1973, she was engaged in research in the field of silicon devices such as high-power p-i-n diodes, high Q varacter diodes, and lately, millimeter wave device technology. She is the holder of several U.S. patents and the author of several technical publications.

Walter Janton served in the U.S. Army as a Communications Technician from 1939 to 1945. In 1948 he graduated from the Baronian School of Horology, Philadelphia PA. From 1953 to 1959 he was a Senior Research Technician at Bell Telephone Laboratories, Murray Hill, NJ in the Model Tube Laboratory. In 1959 he transferred to SFD Research Laboratory (Varian Associates). He joined RCA Laboratories in Princeton, NJ in 1972 as a Research Technician. He has worked on the electron tube injected beam transistor program and cathode-luminescent display devices. For the past three years, he has been responsible for the mechanical design and fabrication of work on the millimeter-wave, p-i-n, and varactor diode projects.

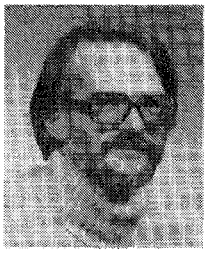
Chung P. Wu (M'74) received the B.S., M.S., M.Phil., and Ph.D. degrees in physics from Yale University in 1965, 1966, 1967, and 1968, respectively.

He was a research staff physicist at the Yale Electron Linear Accelerator Laboratory from 1968 to 1970, working on photonuclear reactions and neutron time-of-flight spectroscopy. From 1970 to 1972 he was an Assistant Professor of Physics at Nanyang University in Singapore. Since 1973, Dr. Wu has been a Member of Technical Staff at RCA Laboratories, Princeton, NJ. He has worked on different techniques for determining the electrically active ion-implanted doping profiles, the utilization of ion implantation in the fabrication of semiconductor devices, and the characterization and evaluation of such devices. He is currently working on the laser annealing of semiconductor materials, including polysilicon, crystalline silicon, SOS, and GaAs, for the fabrication of solar cells, devices, and circuits.

Dr. Wu has more than 20 technical publications and 15 patents granted or pending. He is a member of the American Physical Society and Sigma Xi.

John F. Corboy is an Associate Member of the Technical Staff at RCA's David Sarnoff Research Center, Princeton, NJ, and is a member of the Materials Synthesis Group within the Materials and Processing Research Laboratory. He joined RCA in 1959 and was engaged in the epitaxial growth of III–V compounds and also in the synthesis and crystal growth of organic compounds. From 1965 to 1980 he studied the properties of silicon on insulating substrates and was involved in the transfer of silicon-on-sapphire technology between RCA Laboratories and other divisions of RCA. Currently he is involved in silicon homoepitaxy and plasma etching of oxide films. He has coauthored several publications as well as many internal publications pertaining to silicon on insulators and related subjects.

Mr. Corboy has been issued two U.S. patents and was the recipient of an individual RCA Laboratories Achievement Award in 1974 and a team Achievement Award in 1981.



Charles W. Magee was born in 1947 and was graduated by the Universtiy of Virginia with the B.S. degree in chemistry in 1969, and with Ph.D in 1973. While in graduate school, he concentrated on the electrical methods of ion detection in spark-source mass spectrometry. He was also involved in the development of new types of ion sources for the mass-spectrometric analysis of solids.

He joined the Technical Staff of RCA Laboratories immediately upon completion of his graduate work and is presently a member of the Materials Characteriza-

tion Research Group. His work deals mainly with the trace-elemental analysis of thin solid films by means of secondary-ion mass spectrometry and spark-source mass spectrometry.

Dr. Magee is an active member of the American Society for Mass Spectrometry, having presented numerous technical papers at its National meetings. He is also a member of the steering subcommittee for the Solids and Surface Analysis Committee of the ASMS. In addition, he is a member of the American Vacuum Society and serves on the steering committee for the Greater New York Chapter of the AVS. He is also a member of Sigma Xi.

Specific Equations for One and Two Section Quarter-Wave Matching Networks for Stub-Resistor Loads

RALPH LEVY, FELLOW, IEEE, AND JOSEPH HELSZAJN, MEMBER, IEEE

Abstract—**Given a load network consisting of a conductance in parallel with a short-circuited stub, the admittance values of optimum one and two section commensurate transmission line matching networks are derived. These values are expressed in closed form as functions of the bandwidth and ripple level. It is shown that optimum networks have nonzero reflection coefficient minima, as predicted by classical broad-band matching theory.**

I. Introduction

A CLASSIC PROBLEM in microwave engineering is the broad-band matching of a one-port network consisting of a conductance shunted by a short-circuited stub. A typical example is encountered in the matching of junction circulators. A convenient form of matching network consists of one or more equal length (i.e., commensurate) transmission lines. Several authors have described solutions for the general case having n such lines, the most general result being presented in [1]. A schematic diagram of the network is shown in Fig. 1. It should be noted immediately that this particular form of matching network is not necessarily optimum in having the maximum "gain-bandwidth" product for a given length, but it may be the most convenient for a practical situation. A more optimum network for a similar distributed load network is given in [2], but this is not necessarily so from a practical point of view where realizable impedance levels are a prime consideration.

Papers on matching networks have fallen into two categories. The first consists of sophisticated general solutions

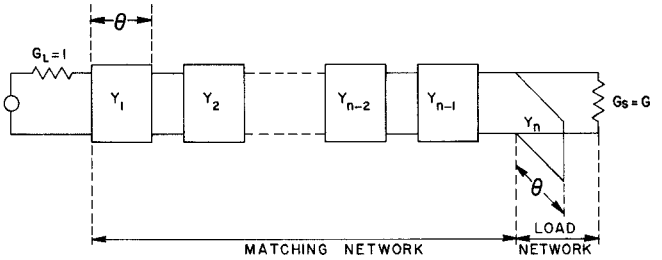


Fig. 1. The general $(n-1)$-section matching network.

such as [1], [2], which have found limited use because of their complexity, not readily appreciated by or comprehensible to a majority of engineers. Included would be the classic papers by Fano [3] and Youla [4]. In the second category are papers which take a more elementary approach, usually involving analysis of one or two section matching networks, leading to results suitable for practical applications, [5], [6]. These methods involve either approximations or solutions to complicated nonlinear simultaneous equations, so that in one sense they are actually more complex than the papers of category 1.

One object of this paper is to demonstrate that the classical ("sophisticated") synthesis method of category 1 is actually simpler than the direct ("brute force") method of category 2 when applied to equally simple networks, i.e., with one or two matching elements rather than the general n-element case. Specific equations for the elements of the matching networks result, and computer-derived solutions are not required.

A second objective is to solve the matching problem for the general case where the reflection coefficient minima take on finite values rather than zero. This gives improved

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